REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 are pending in the present application. Claims 1, 2, 9 and 10 are amended by the present amendment.

This amendment is submitted in accordance with 37 C.F.R. § 1.116, which after final rejection permits entering of amendments, canceling claims, complying with any requirement of form expressly set forth in a previous Office Action, or presenting rejected claims in better form for consideration on appeal. It is therefore respectfully requested that the present amendment be entered under 37 C.F.R. § 1.116.

In the outstanding Office Action, the title was objected to; Claims 1-15 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 2, 5-10 and 13-15 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,006,980 to Sanders; and Claims 3, 4, 11 and 12 were rejected under § 103(a) as unpatentable over Sanders in view of U.S Patent No. 6,477,638 to Gearty and Hennessy, "Computer Organization and Design."

Regarding the objection to the title, the title is amended as suggested in the outstanding Office Action. Accordingly, Applicant respectfully requests the objection to the title be withdrawn.

Further, regarding the rejection of Claims 1-15 under 35 U.S.C. § 112, second paragraph, Claims 1, 2, 9 and 10 are amended in light of comments in the outstanding Office Action. Accordingly, Applicant respectfully requests the rejection of Claims 1-15 under 35 U.S.C. § 112, second paragraph, be withdrawn.

In addition, Applicant respectfully traverses the rejection of Claims 1, 2, 5-10 and 13-15 under 35 U.S.C. § 102(e) as anticipated by Sanders.

Amended Claim 1 is directed to a data processing apparatus configured to perform a pipeline processing by dividing a pipeline into a plurality of stages. The data processing apparatus includes a first pipeline processing portion that performs the processing in a plurality of stages in sequence based on a plurality of control signals provided corresponding to the respective stages. The control signals having timings capable of being individually controlled. The data processing apparatus also includes a first latch portion that latches the control signal inputted to each stage with a predetermined clock. The first latch portion has flip-flops which are provided corresponding to the respective control signals and which latch the corresponding control signal. In addition, the data processing apparatus includes a second pipeline processing portion, disposed separately from the first pipeline processing portion. The second pipeline processing portion performs the processing in each stage based on the control signal latched by the first latch portion.

Thus, the first pipeline processing portion is controlled by a plurality of control signals provided with the respective stages, and the second pipeline processing portion is controlled based on the signals latched by the flip-flops corresponding to the control signals.

By providing the control signals individually for the respective stages, the claimed invention accurately controls operational timing at each stage, thereby promptly filling vacancies in the pipelines. Accordingly, it is possible to perform pipeline processing at high speed.

Furthermore, the second pipeline processing portion is controlled with the signal latched by the flip-flops corresponding to the control signals. Therefore, the processing of the second pipeline processing portion can be executed one cycle later than that of the first pipeline processing portion. Hence, according to the invention of Claim 1, it is possible to execute the processings of the pipeline processing portions by staggering the processing time of each pipeline processing portion with respect to another pipeline processing portion.

In other words, in the claimed invention, a plurality of control signals having different types are provided for the respective stages. Therefore, it is possible to accurately control the timing at each stage. That is, the operational timing at a certain stage does not depend on the operational timing at the other stages.

Further, the flip-flops are provided to latch the control signals to set the operational timing at each stage. Thus, the first pipeline processing portion does not operate in sync with the outputs of the flip-flops, but operates based on the control signals.

Applicant respectfully submits that Sanders does not teach or suggest features of the claimed invention. Sanders shows latches for respective stages in Fig. 12. Sander's latches are connected in series, the control input 28 is input to the latch at an initial stage, and the outputs of the latches control the segments in the execution unit and the memory management unit. Thus, Sanders describes only one type of control input (i.e., control input 28), which is applied to both the execution unit and the memory management unit. Hence, Sanders does not teach or suggest "control signals having timings capable of being individually controlled," as recited in amended independent Claim 1 and as similarly recited in amended independent Claim 9.

Further, Sanders indicates that each pipeline stage is controlled with the signal obtained by sequentially latching the control input 28. That is, each stage in Sanders operates depending on the timing of the common control input 28, which is different than the claimed invention which applies the control signals to the respective units. Hence, Applicant respectfully submits that Sanders does not teach or suggest "a first latch portion configured to latch said control signal inputted to each stage with a predetermined clock, said first latch portion having a plurality of flip-flops which are provided corresponding to the respective control signals and latch the corresponding control signal; and a second pipeline processing portion, disposed separately from said first pipeline processing portion, configured to perform

the processing in each stage based on the control signal latched by said first latch portion, as recited in amended Claim 1 and as similarly recited in amended independent Claim 9.

Accordingly, Applicant respectfully submits independent Claims 1 and 9, and claims depending therefrom, are allowable.

In addition, Applicant respectfully traverses the rejection of Claims 3, 4, 11 and 12 under 35 U.S.C. § 103(a) as unpatentable over Sanders in view of Gearty and Hennessy.

Applicant respectfully submits that the disclosure of Gearty and Hennessy do not teach or suggest the features of the claimed invention. Gearty shows two pipelines and a latch circuit in Fig. 4. However, Gearty neither discloses nor suggests that the control signals are provided to the respective stages. Although Gearty uses the output of stage F3 as the control signal, there is no other control signal, and thus Gearty is different than the claimed invention, which includes control signals provided to the respective stages. Further, Applicant respectfully submits that Hennessy also does not teach or suggest the claimed features lacking in the disclosures of Gearty and Sanders.

Accordingly, Applicant respectfully requests the rejection of Claims 3, 4, 11 and 12 under 35 U.S.C. § 103(a) be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action that effect is respectfully requested.

Respectfully submitted,

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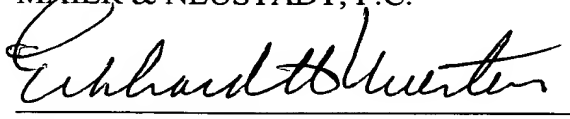
MAIER & NEUSTADT, P.C.



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